IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Art Unit: 2892
Examiner: Mr. William F. Kraig

In re PATENT APPLICATION of:

Applicant	:	Akira TAKAHASHI	)
Serial No.	:	10/798,482	)
Filed	:	March 12, 2004	)
For	:	DRY ETCHING METHOD FOR SEMICONDUCTOR DEVICE	)
Attorney Ref.	:	OKI 414	)

PETITION

April 21, 2009

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is a Petition to seek review of objections that are set forth in sections 3 and 4 of an Office Action dated January 21, 2009.

BACKGROUND

Procedurally, these objections are rose as follows: An Office Action dated October 22, 2007 objected to the drawings on the ground that they failed to show every feature that is specified in the claims. In response, an Amendment that was filed on March 24, 2008 forwarded a replacement drawing sheet for Figures 3(a)-3(c) and a new Figure 4. Several modifications were presented in the replacement sheet for Figures 3(a)-3(c), but the main issue involves the addition of a dummy gate arrangement 9 in Figure 3(c), and also new Figure 4 (which also shows the dummy gate arrangement 9). The Amendment of March 24, 2008 also modified the specification to refer to the dummy gate arrangement 9.

An Office Action dated June 9, 2008 objected to the Amendment of March 24, 2008 on the ground that the revisions to Figure 3 and the addition of new Figure 4, along

with the revision to the specification concerning the dummy gate arrangement 9, constituted new matter. The Office Action required cancellation of the alleged new matter.

An Amendment filed on October 31, 2008 traversed the objections to the drawings and specification. The traverse was not successful, since section 4 of the Office Action of January 21, 2009 objects to the Amendment filed on March 24, 2008 and requires cancellation of the alleged new matter in the drawings and specification.

ARGUMENT

The present application discloses a technique for confronting a problem that arises when N type polysilicon gate electrodes and P type polysilicon gate electrodes are etched simultaneously. The problem is illustrated in Figure 2 of the application's drawings, which shows that some of the gate electrodes are over-etched, resulting in gate electrodes that are tapered by the time other gate electrodes are completely etched. The solution to this problem is summarized in the paragraph bridging pages 4 and 5 of the present application. This paragraph stages, "The present invention aims to provide a semiconductor device comprising an N type polysilicon gate and a P type polysilicon gate both disposed simultaneously, wherein a dummy gate made of non-doped polysilicon is disposed for polysilicon gate etching and set so as to take an area larger than the total area of the N type polysilicon gate and the P type polysilicon gate ...".

In the original version of Figures 3(a)-3(c), phosphor ions are implanted into a region 4 for forming an N type gate electrode and boron ions are implanted into a region 5 for forming a P type gate electrode. No impurities are injected into a dummy gate electrode region 6. Subsequent processing results in gate electrodes as shown in Figure 3(c), but a dummy gate electrode is not shown in the original version of Figure 3. It is Applicant's position that an ordinarily skilled person who had read the present application would have realized that a dummy gate electrode should be shown in Figure 3(c), in the dummy gate electrode region 6, and that an ordinarily skilled person who had read the application as-filed would have realized that the inventor was in mental possession of the alleged new matter. However, section 4 of the Office Action of January 21, 2009 asserts that "there is nothing in the original disclosure which supports there being structure remaining in the non-doped polysilicon region after the described etching process." Applicant respectfully disagrees with this assertion.

The preset application discloses that P type polysilicon and N type polysilicon etch at different rates (see, for example, the paragraph bridging pages 2 and 3 of the application and the paragraph bridging pages 7 and 8). The application also discloses that non-doped polysilicon etches at a rate which lies between the etching rate of P type polysilicon and N type polysilicon (see the paragraph at page 7 of the application, lines 14-25). Since both a P type polysilicon gate electrode and an N type polysilicon gate electrode are shown in original version of Figure 3(c), what the application calls a "dummy gate" of non-doped polysilicon should also be present in Figure 3(c), within the region identified as dummy gate electrode region 6 in Figure 3(b).

Furthermore, although the drawings do not show a mask with patterns for etching the N type and P type gate electrodes that are shown in the original version of Figure 3(c), an ordinarily skilled person would have understood that a mask is used to permit etching of these gate electrodes. The application advises that dummy gate patterns are disposed on the mask (see page 7, lines 3-7). An ordinarily skilled person would have realized that the result would be a dummy gate electrode in Figure 3(c), as in the replacement drawing sheet that was forwarded with the Amendment filed on March 24, 2008.

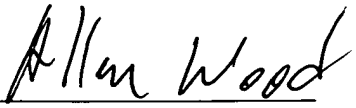
The application discloses that the dummy gate has an area larger than the total area of the N type polysilicon gate and the P type polysilicon gate (see the paragraph, noted above, bridging pages 4 and 5 of the application). This is what is shown in new Figure 4.

The new matter allegedly added to the specification includes the following sentence that was modified by the Amendment filed on March 24, 2008: "Subsequently, patterning is done by a lithography technique and the ~~non-doped polysilicon and~~ doped polysilicon regions 4 and 5 [[in]] and the dummy gate electrode region 6 are etched to form gate electrodes 7 and 8 and a dummy gate arrangement 9 (see Fig. 3(c))." The alleged new matter added to the specification also includes the following modification that was presented in an Amendment filed on April 27, 2006: "Fig. 3(c) shows that the area occupied by the etched non-doped polysilicon ~~region 6~~ dummy gate pattern is larger than the total area occupied by the N-type and P-type polysilicon ~~regions~~ gates which have been etched." From the above discussion of the drawing changes, it will be apparent that these modifications to the specification were within the mental possession of the inventor at the time this application was filed.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner should be directed to withdraw the new matter objections to the drawings and specification.

Respectfully submitted,



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